REMARKS

Before this Reply, Claims 1-27 were pending in the above-referenced patent application. Through this Reply, new Claims 28-42 have been added. New Claims 28-42 are supported by the specification. Claims 19, 22, 23 and 27 have been amended to correct typographical errors. Further, Claims 5, 6, 12, 13, 14 and 21 have been amended to further clarify the claimed limitations. No new matter has been added. Entry and consideration of the amendments and the new claims are respectfully requested.

All of Claims 1-27 were rejected under 35 U.S.C. 103(a). Specifically, Claims 1, 2, 10, 11, 18 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 6,618,788 to Jacobs in view of prior art. Claims 3, 7, 15, 22 and 23 were rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobs in view of USB Specification 2.0. Claims 4-6, 9, 12-14, 20 and 21 were rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobs in view of USPN 6,131,134 to Huang et al. ("Huang"). Claims 8, 16, 17 and 24-27, were rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobs in view of USB Specification 2.0, and further in view of Huang. All of the rejections are respectfully traversed because the references, alone or in combination, do not disclose all of the claimed limitations. No prima facie case of obviousness has been established.

As per Claim 1, despite the Examiner's interpretation, Jacobs (col. 5, lines 29-33, relied on by the Examiner) does not disclose a USB system for data communication between a processor and IDE devices, comprising a plurality of IDE devices, and a plurality of USB-to-IDE bridges, wherein each IDE device is connected to a respective USB-to-IDE bridge, as required by Claim 1. Instead, in col. 5, lines 29-33, Jacobs simply states: "And although the following discussion will focus on a single ATA DEV0, ATA device 140 could also incorporate two physical devices, one functioning as DEV0 and the other as DEV1 on the same ATA bus." Jacobs mentions that the

ATA device 140 (Fig. 5) can incorporate two devices *functioning on the same ATA bus in the device 140*. One of the devices in the device 140 functions as DEV0 and the other as DEV1 on the same ATA bus in device 140. Jacobs does not disclose a plurality of IDE devices, each coupled to a IDE-to-USB bridge that is connected to a USB controller, as required by Claim 1 (i.e., Jacob's devices DEV0 and DEV1 function on an ATA bus in the device 140 that is connected to the cabling bridge 156). Indeed, Even if Jacobs utilizes two devices DEV0 and DEV1 in the ATA device 140, Jacobs still uses only one USB-to-ATA bridging cable 156 for the two devices DEV0 and DEV1, not a plurality of USB-to-IDE bridges corresponding to a plurality of IDE devices, as required by Claim 1.

In addition, as Jacobs clearly specifies, the element 130 is a host machine, and not a USB controller as required by Claim 1. Further, Jacobs does not disclose a USB controller, wherein the USB-to-IDE bridges are connected to the USB controller, whereby the processor can communicate with the IDE devices via the USB controller. Nor does Jacobs mention a USB controller than can be connected to multiple USB-to-IDE bridges for communication therewith. For at least these reasons, rejection of Claim 1, and all claims dependent therefrom should be withdrawn.

Claims 10 and 18 were rejected for substantially the same reasons as rejection of Claim 1. As such, for at least the reasons provided above in relation to Claim 1, it is respectfully submitted that rejection of Claims 10, 18, and all claims dependent therefrom, should be withdrawn.

As per Claim 4, as the Examiner also states, Jacobs does not disclose a system wherein a IDE device can be utilized in hot plugging. The Examiner states that Huang discloses such a feature, and that it would have been obvious to modify Jacobs according to Huang to achieve the claimed invention. However, Huang is directed to USB converter working between an old interface (legacy interface) and a USB interface, to enable the hot PnP function on the system (col.

3, lines 1-3; col. 5, lines 30-33). Huang's USB converter inputs legacy interface (non USB) signals and outputs USB signals. The USB converter of Huang is incompatible with Jacobs' smart cable 150 (Jacobs, Fig. 5). In Fig. 5 of Jacobs, Huang's USB converter cannot be connected between the smart cable 150 and the USB port 132. The USB plug 154 of Jacobs' cable 150 is already in USB format, not legacy format as Huang requires, and as such it is incompatible with input to Huang's USB converter. Nor can Huang's USB converter be connected between the ATA device 140 and the ATA connector 152 because Huang's USB connector outputs USB signals but the connector 152 expects ATA signals. A combination of Jacobs and Huang is non-functional. Further, neither of the references provides a motivation for a combination thereof. For at least these reasons, rejection of Claim 4 should be withdrawn.

As per Claims 7, 15, 22, neither Jacobs nor Huang provide any motivation of utilizing a USB hub, and neither disclose that such a feature would even work with their system. Therefore, it is respectfully requested that rejection of Claims 7, 15, 22, and all claims dependent therefrom, should be withdrawn.

Rejection of Claims 5, 6 and 9 is respectfully traversed for at least the reasons provided in relation to Claim 5. Further, as per Claim 6, Jacobs (col. 1, lines 49-51), only allows up to two ATA devices (e.g., devices 44 and 46 on FIG. 1) to share the ATA bus 42. As such, only up to two devise can be incorporated in the device 140, connected to one cable 150.

Claims 12, 13, 14, 20 and 21 were rejected for substantially the same reasons as rejection of Claims 5, 6 and 9, and should therefore be allowed for at least the reasons provided in relation to Claims 1, 5, 6 and 9. Further, rejection of Claims 8, 16, 17, 24-27 should be withdrawn for at least the reasons provided in relation to Claims 1, 5-7, 9, 15 and 22.

CONCLUSION

For the foregoing, and other, reasons Applicants believe that the rejected claims should be allowed. Reconsideration and allowance of the rejected claims are respectfully requested.

Please continue to direct all communications regarding the above-referenced patent application to the principal agent of record.

Respectfully Submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence or paper is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450, on Sept. 16, 2004.

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Michael Zarrabian
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